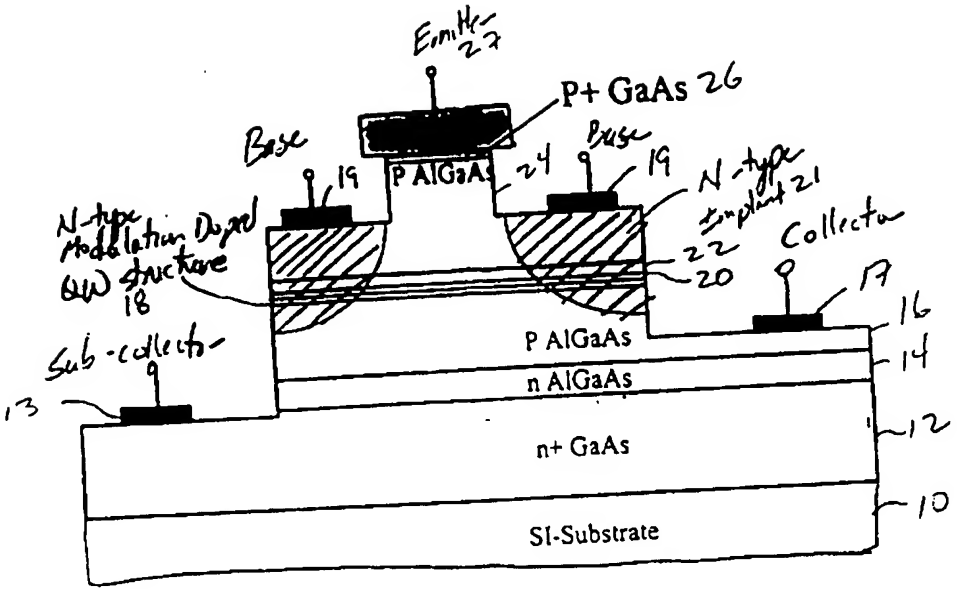

Emitter
27
P+ GaAs 26
Base
19
P AlGaAs
24
Base
19
N-type
implant 21
22
20
Collector
17
16
14
12
10
N-type
Modulation Doped
QW structure
18
Sub-collector
13
P AlGaAs
n AlGaAs
n+ GaAs
SI-Substrate

FIG. 1

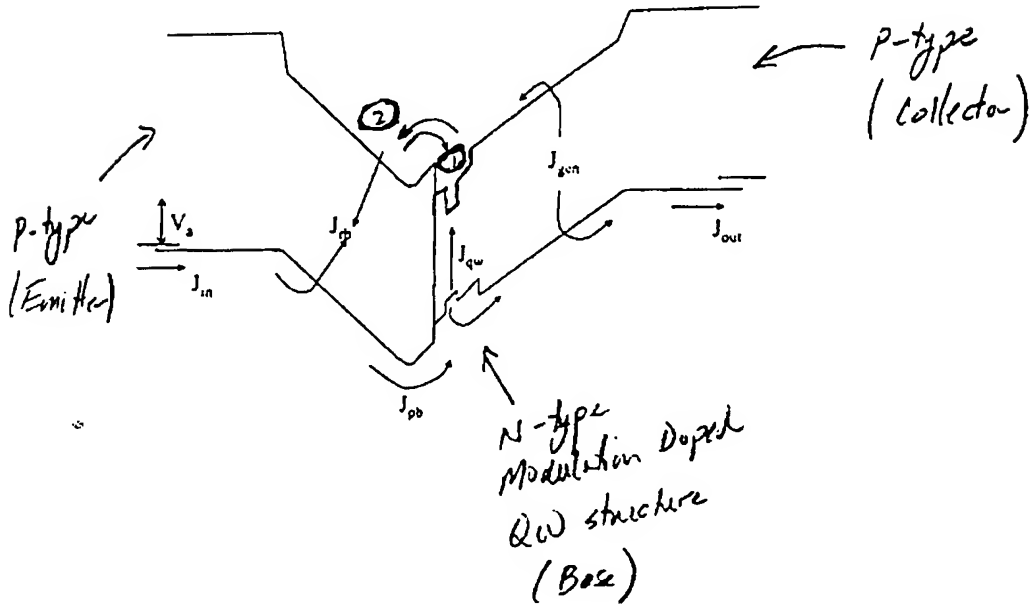

P-type
(collector)
P-type
(Emitter)
V_a
J_{in}
J_{qw}
J_{out}
J_{pb}
N-type
Modulation Doped
QW structure
(Base)

FIG. 2

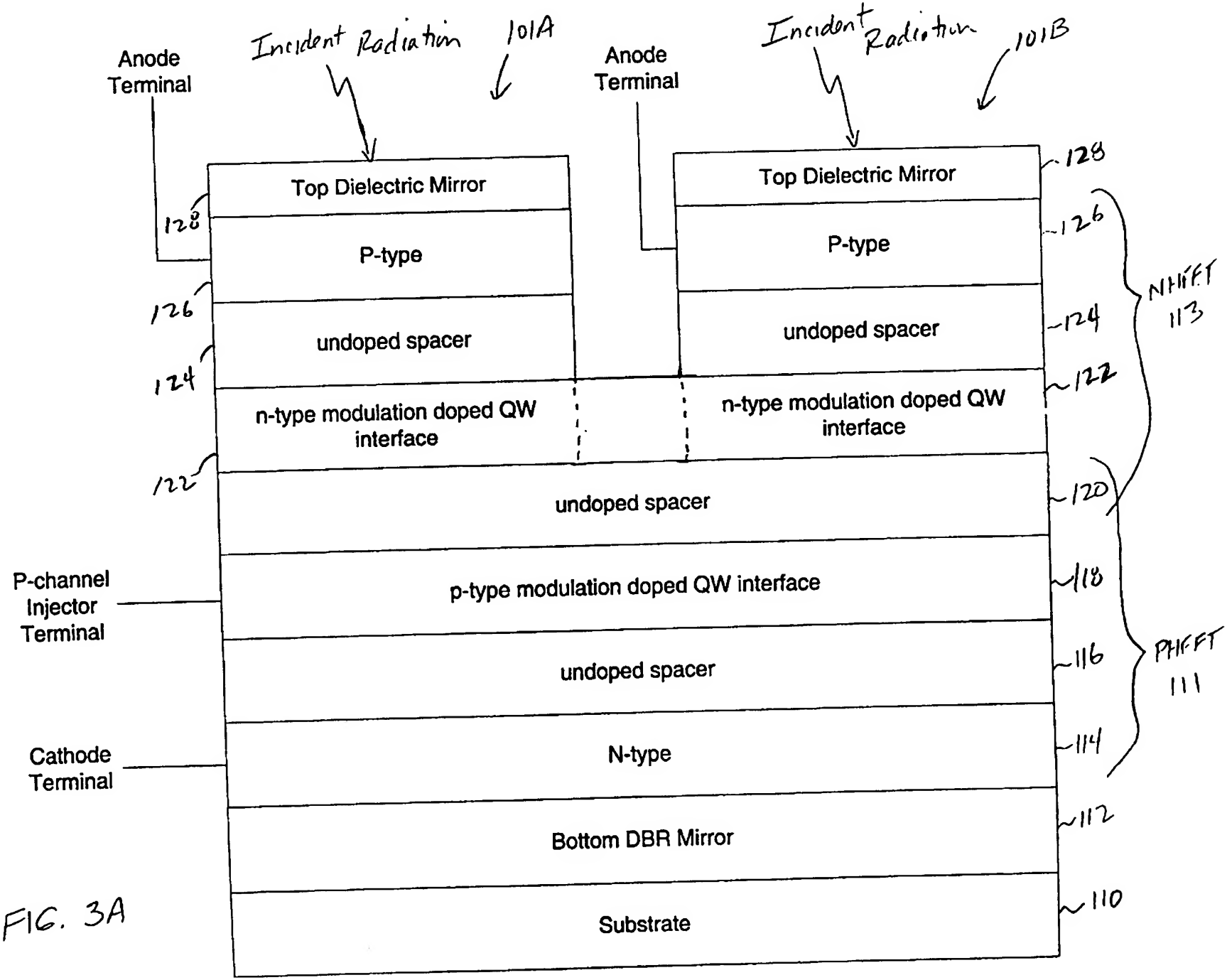

Anode Terminal
Incident Radiation
101A
Anode Terminal
Incident Radiation
101B
Top Dielectric Mirror
128
P-type
126
undoped spacer
124
n-type modulation doped QW interface
122
undoped spacer
120
p-type modulation doped QW interface
118
undoped spacer
116
N-type
114
Bottom DBR Mirror
112
Substrate
110
NHFET 113
PHFET 111
P-channel Injector Terminal
Cathode Terminal

FIG. 3A

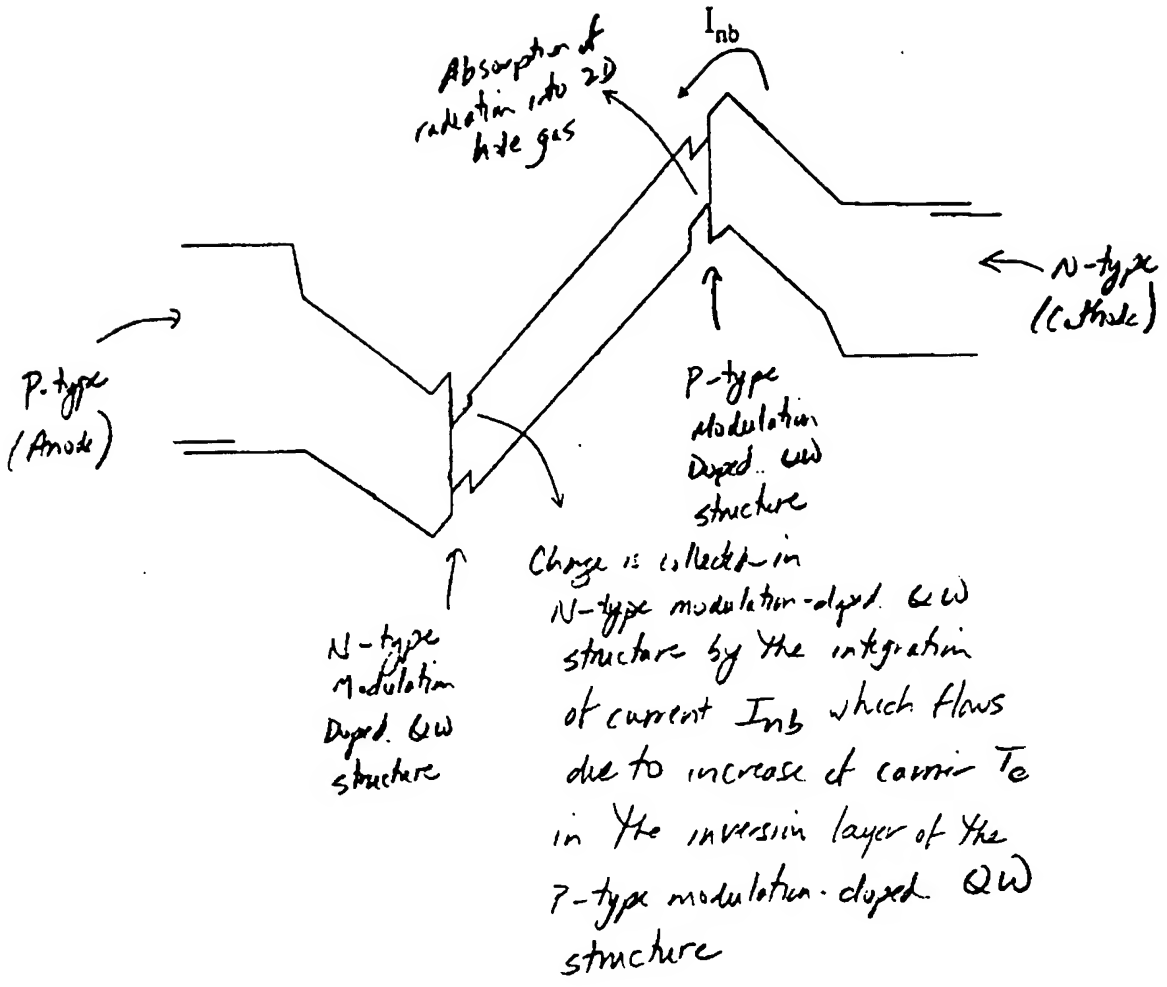

I_{nb}
Absorption of radiation into 2D hole gas
N-type (Cathode)
P-type (Anode)
P-type modulation Doped QW structure
N-type modulation Doped QW structure
Charge is collected in N-type modulation-doped QW structure by the integration of current I_{nb} which flows due to increase of carrier T_e in the inversion layer of the P-type modulation-doped QW structure

FIG. 3B

Pixel Setup Mode

FIG. 4A

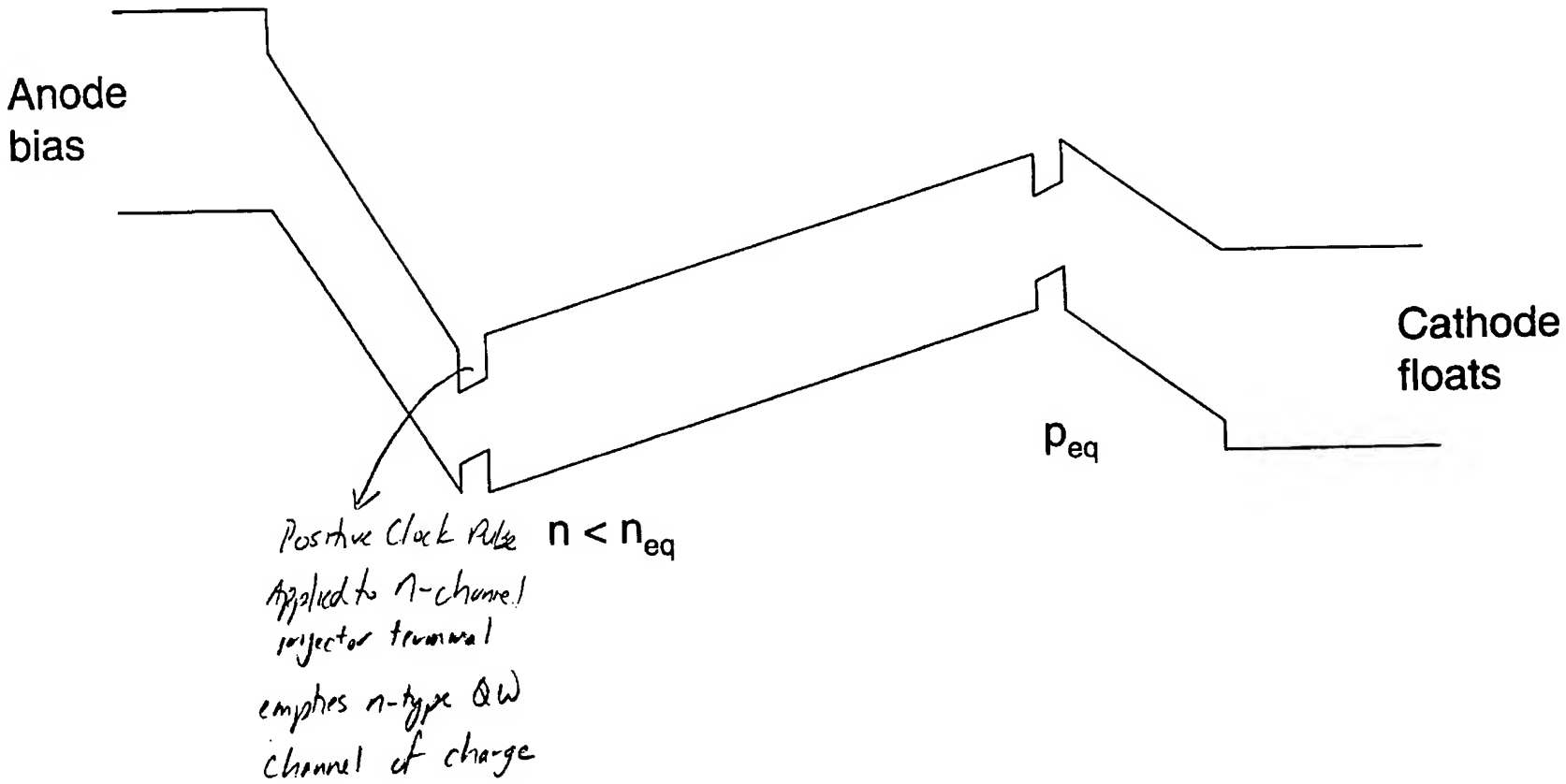


FIG. 4B

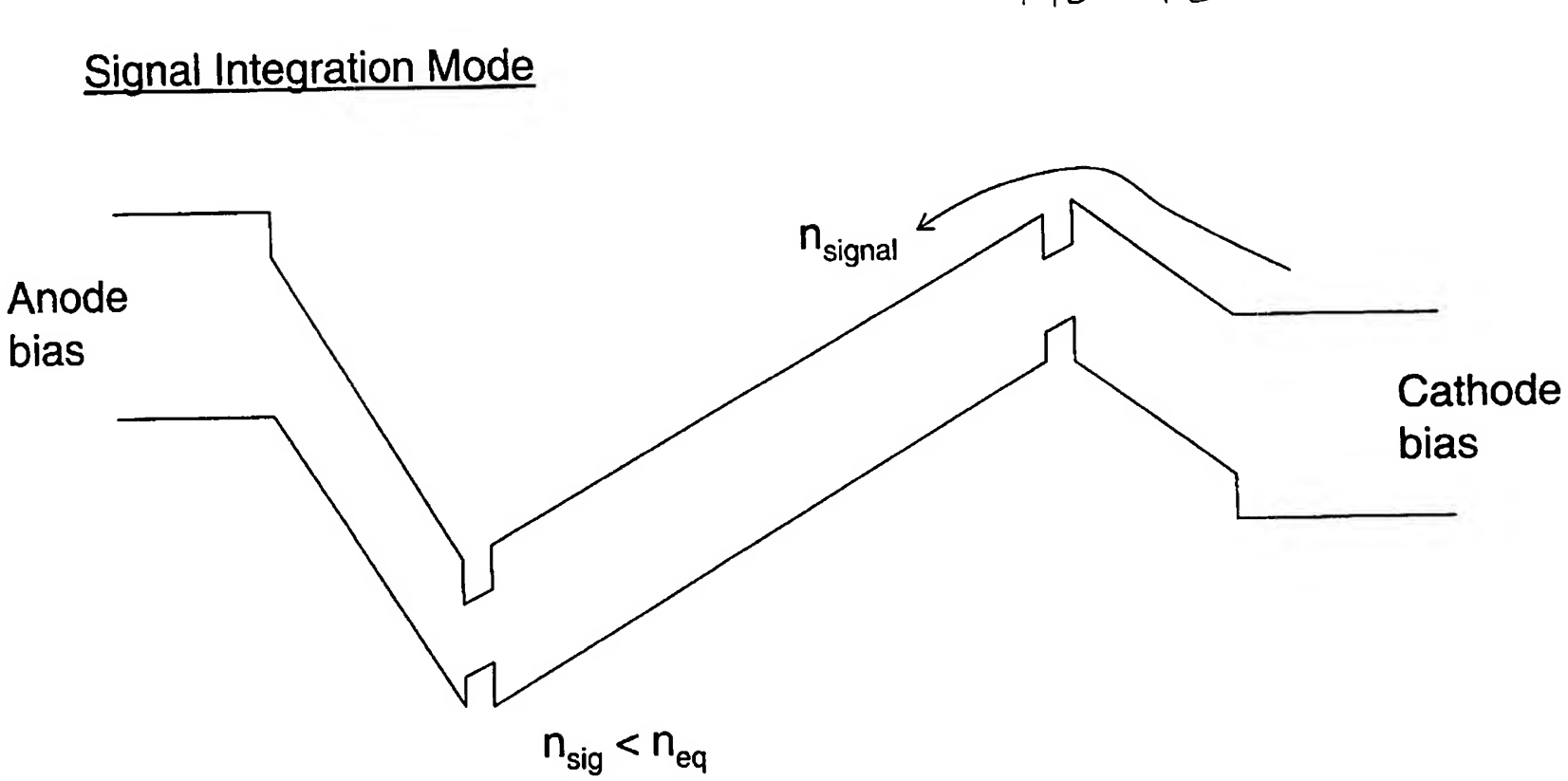
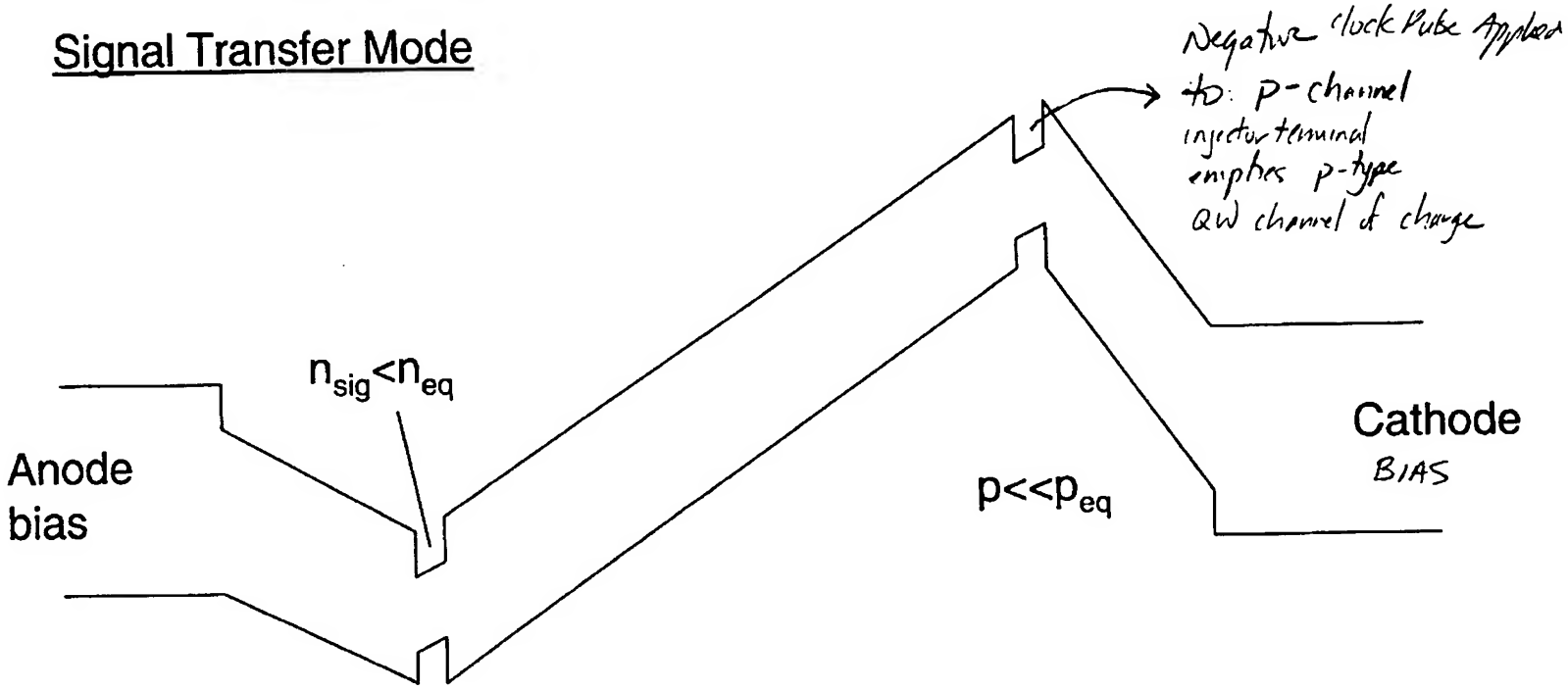

Signal Integration Mode
Anode bias
n_{signal}
Cathode bias
$n_{sig} < n_{eq}$

FIG. 4C


Signal Transfer Mode
Negative clock Pulse Applied to: p-channel injector terminal empties p-type QW channel of charge
$n_{sig}<n_{eq}$
Anode bias
$p<<p_{eq}$
Cathode BIAS

	Layer Material	Layer Doping Type	Typical Doping Concentration (atoms/cm^3)	Typical Layer Thickness (A)	Layer #
126	InGaAs	P+	1E20	25	1165b
	GaAs	P+	1E20	75	1165a
	Al(0.7)Ga(0.3)As	P	1E17	700	1164b
	Al(0.7)Ga(0.3)As	P+	1E19	10	1164a
	Al(.15)Ga(.85)As	P+	3.5E18	25	1163d
124	Al(.15)Ga(.85)As	und	und	200 - 300	1163c
122	Al(.15)Ga(.85)As	N+	3.5E18	80	1163b
	Al(.15)Ga(.85)As	und	und	20-30	1163a
	GaAs	und	und	15	1162
	In(.20)Ga(.80)AsN	und	und	60	1161
	GaAs (x3)	und	und	100	1160b
	GaAs	und	und	100 - 250	1160a
120	Al(.15)Ga(.85)As	und	und	5000	1159
118	GaAs	und	und	100	1158
	In(.20)Ga(.80)AsN (x3)	und	und	60	1157
	GaAs	und	und	15	1156
	Al(.15)Ga(.85)As	und	und	30	1155d
	Al(.15)Ga(.85)As	P+	3.5E18	80	1155c
116	Al(.15)Ga(.85)As	und	und	300	1155b
114	Al(.15)Ga(.85)As	N+	3.5E18	80	1155a
	Al(0.7)Ga(0.3)As	N	1E17	700	1154
	GaAs	N+	3.5E18	2200	1153
112	AlAs	und	und	1701	1151
	GaAs (x 7)	und	und	696	1152
	AlAs	und	und	1701	1151
110	GaAs Substrate		SI		1149

FIG. 5

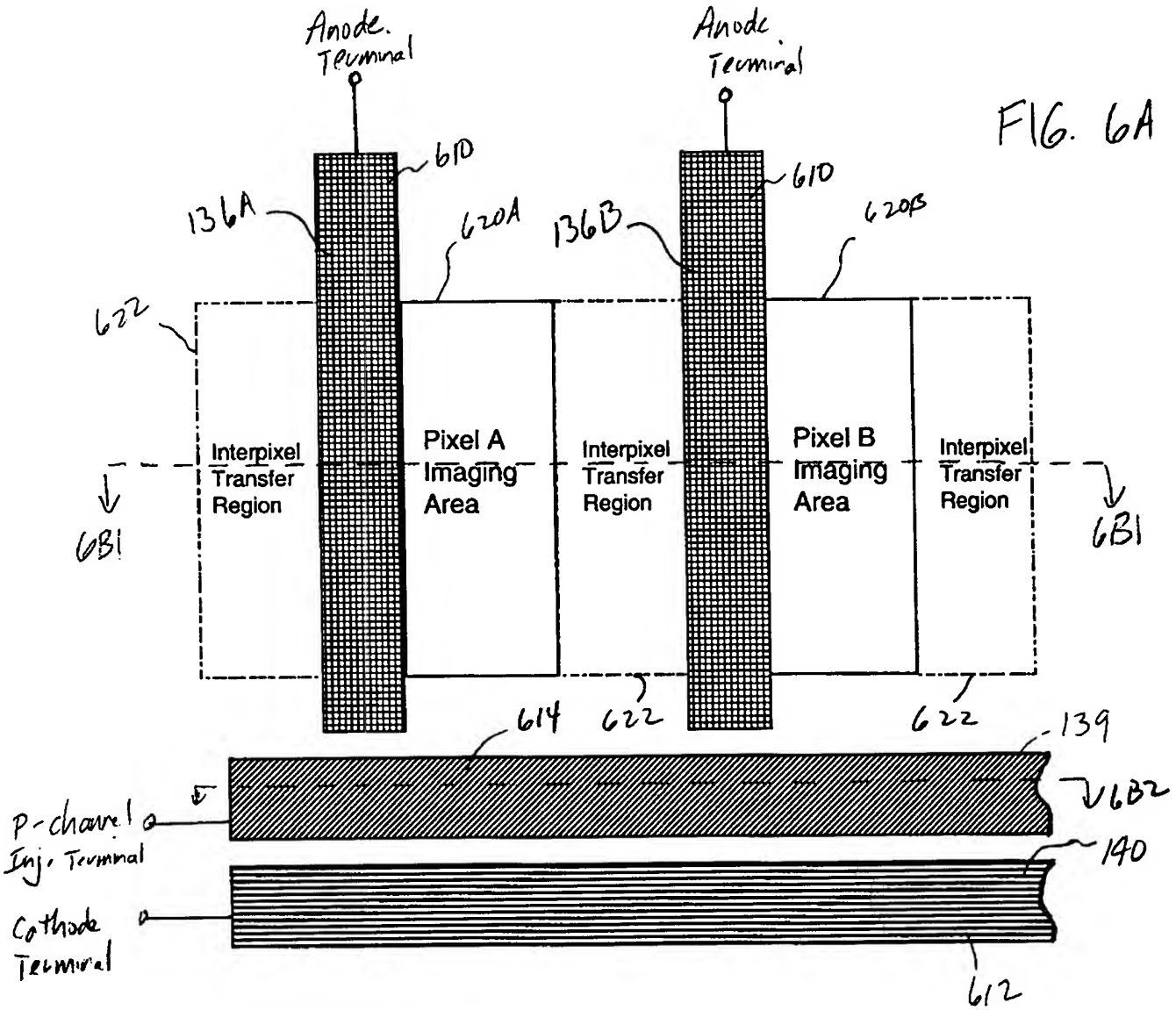

Anode Terminal
Anode Terminal
610
610
136A
136B
620A
620B
622
Interpixel Transfer Region
Pixel A Imaging Area
Interpixel Transfer Region
Pixel B Imaging Area
Interpixel Transfer Region
6B1
6B1
614
622
622
139
6B2
P-channel Inj. Terminal
140
Cathode Terminal
612

FIG. 6A

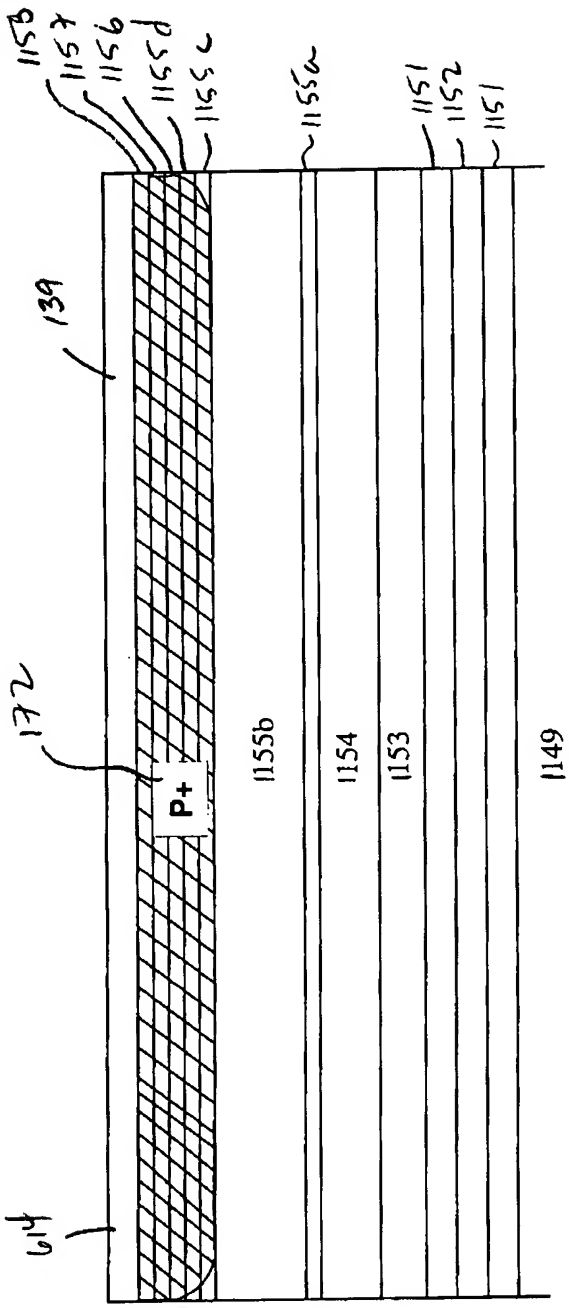

1158
1157
1156
1155
1155a
1155b
1154
1153
1152
1151
1149
139
137
P+

FIG. 6B2

FIG. 6B1

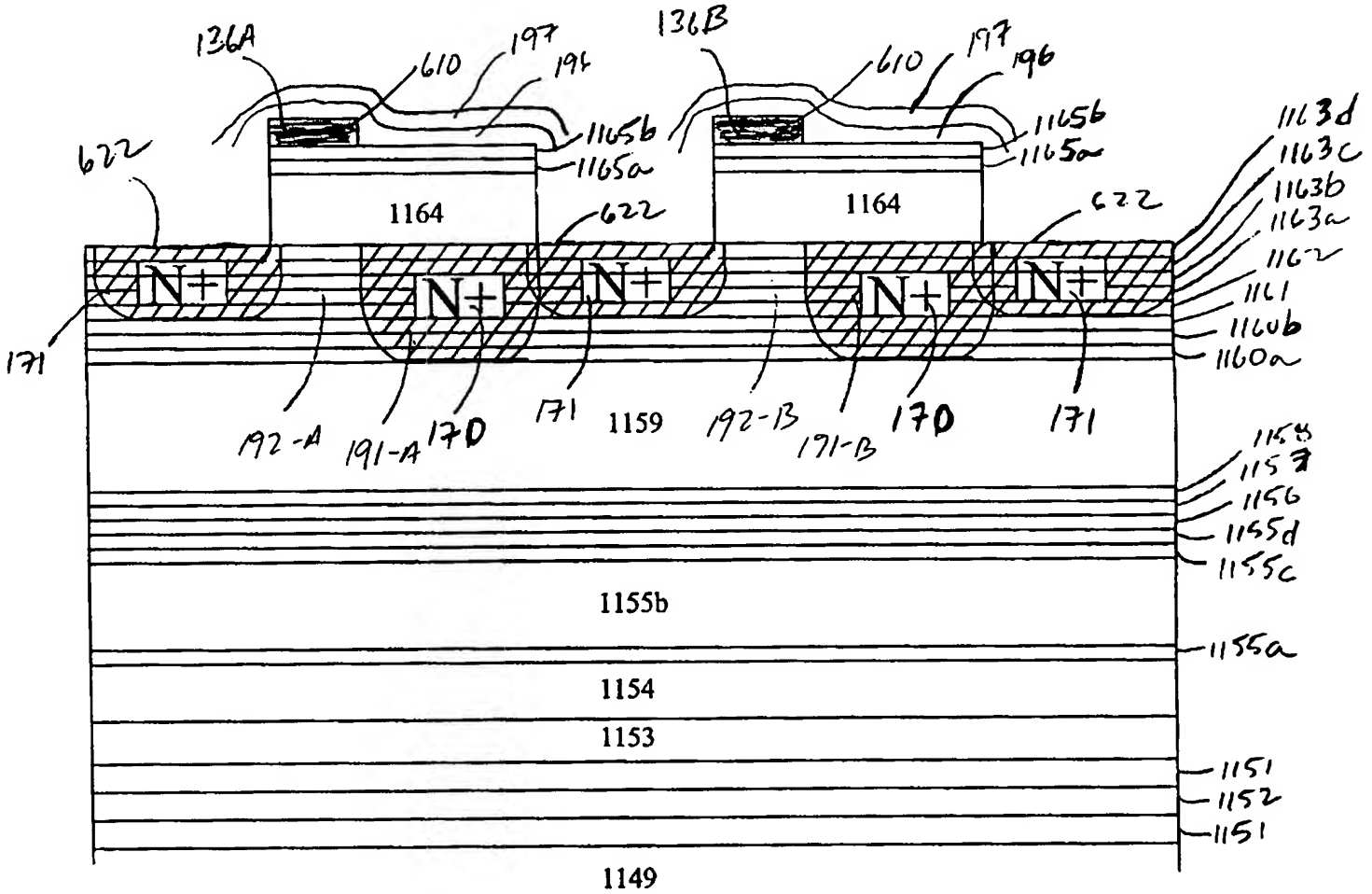
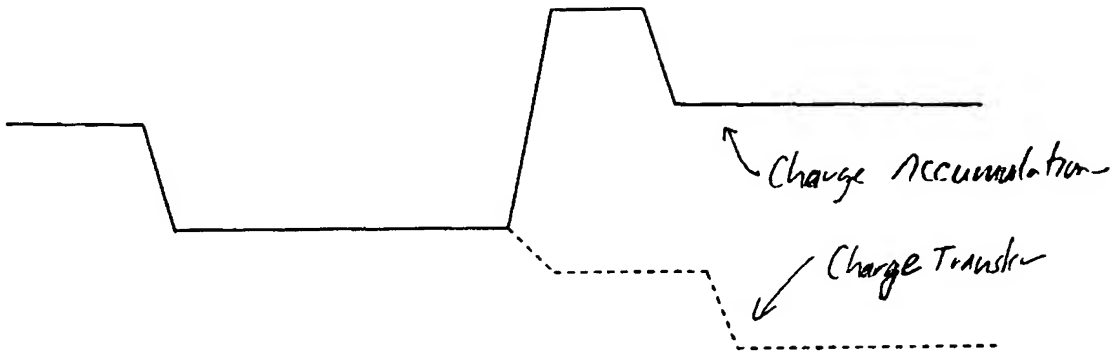


FIG. 6C



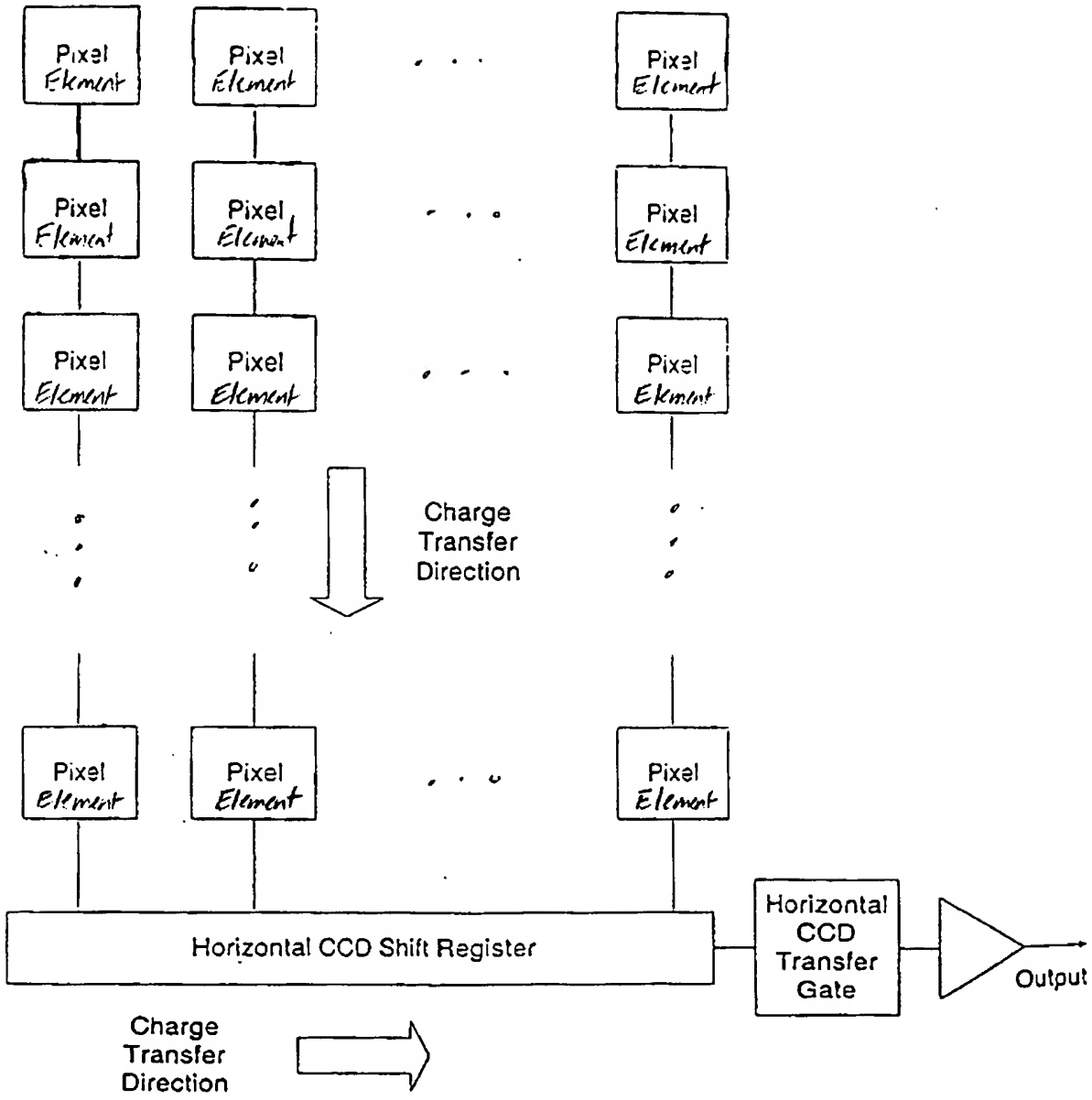

Pixel Element
Charge Transfer Direction
Horizontal CCD Shift Register
Horizontal CCD Transfer Gate
Output
Charge Transfer Direction

FIG. 7A

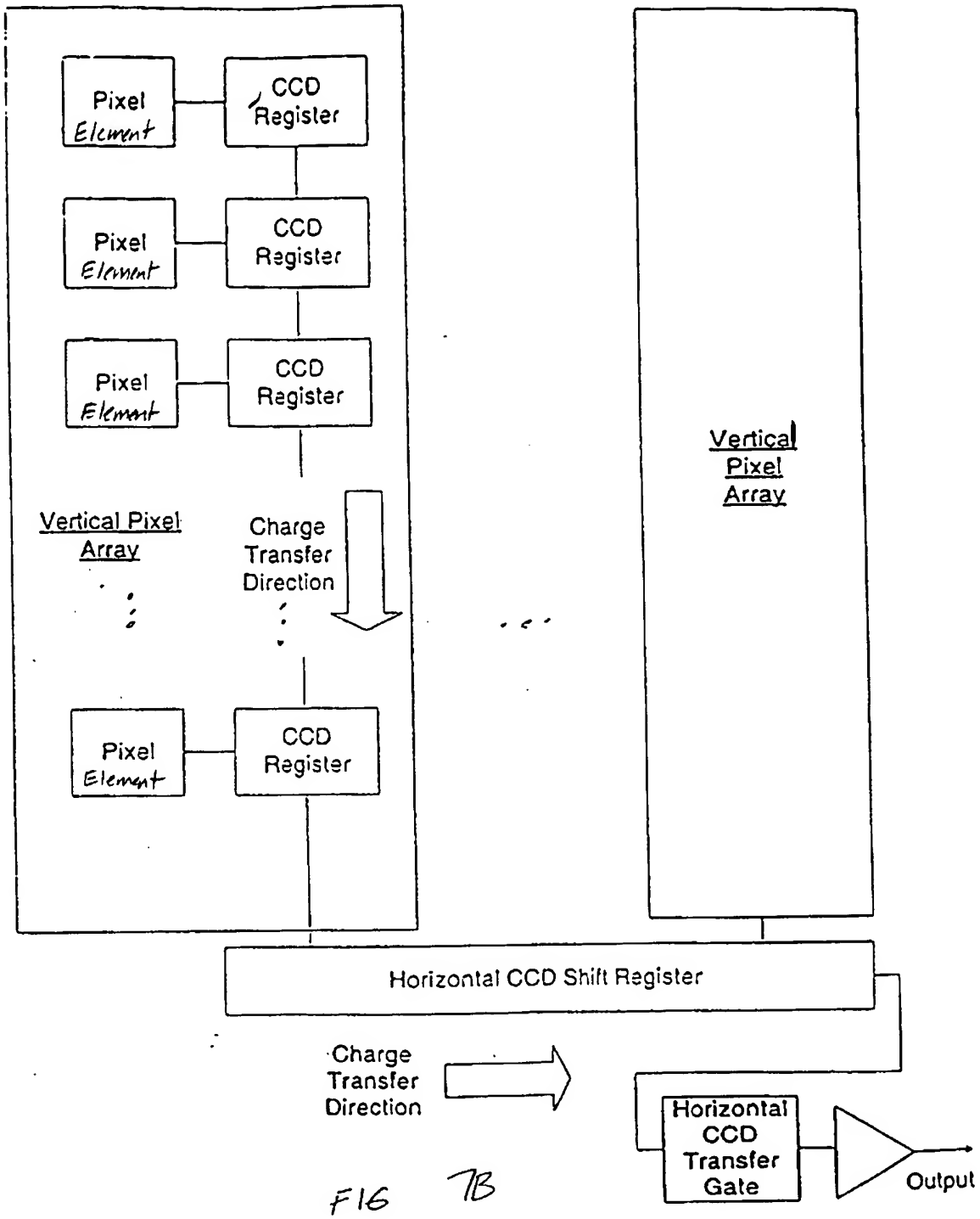

Pixel Element
CCD Register
Pixel Element
CCD Register
Pixel Element
CCD Register
Vertical Pixel Array
Charge Transfer Direction
Pixel Element
CCD Register
Vertical Pixel Array
Horizontal CCD Shift Register
Charge Transfer Direction
Horizontal CCD Transfer Gate
Output

FIG 7B

FIG. 8A

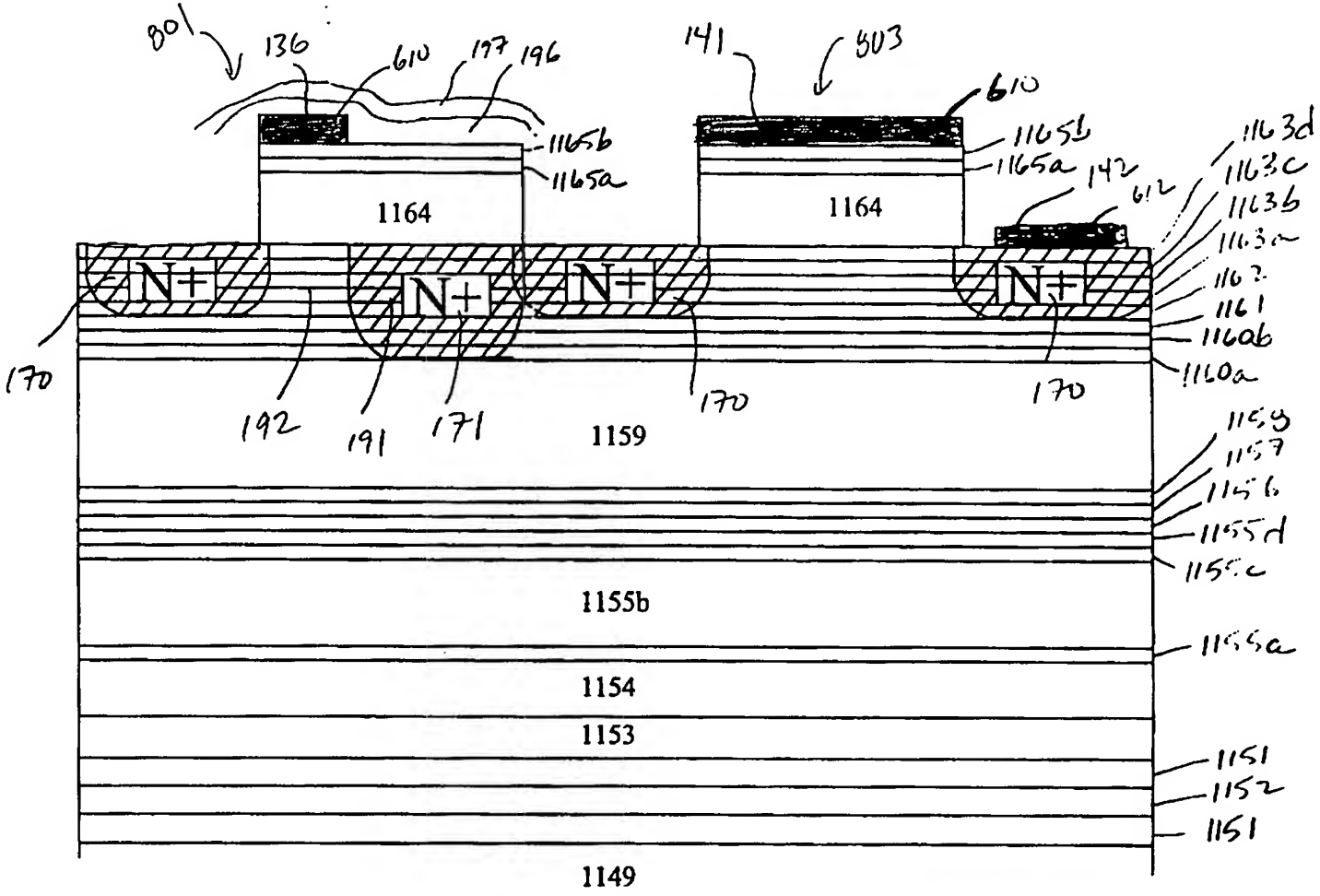
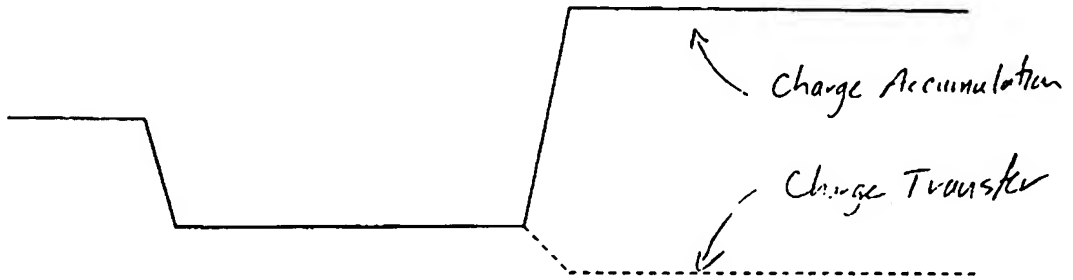

801
136
610
197
196
141
603
610
1165b
1165a
1164
1164
142
612
1163d
1163c
1163b
1163a
1162
1161
1160b
1160a
N+
N+
N+
N+
170
192
191
171
170
170
1159
1155g
1155f
1155e
1155d
1155c
1155b
1155a
1154
1153
1151
1152
1151
1149

FIG. 8B


Charge Accumulation
Charge Transfer

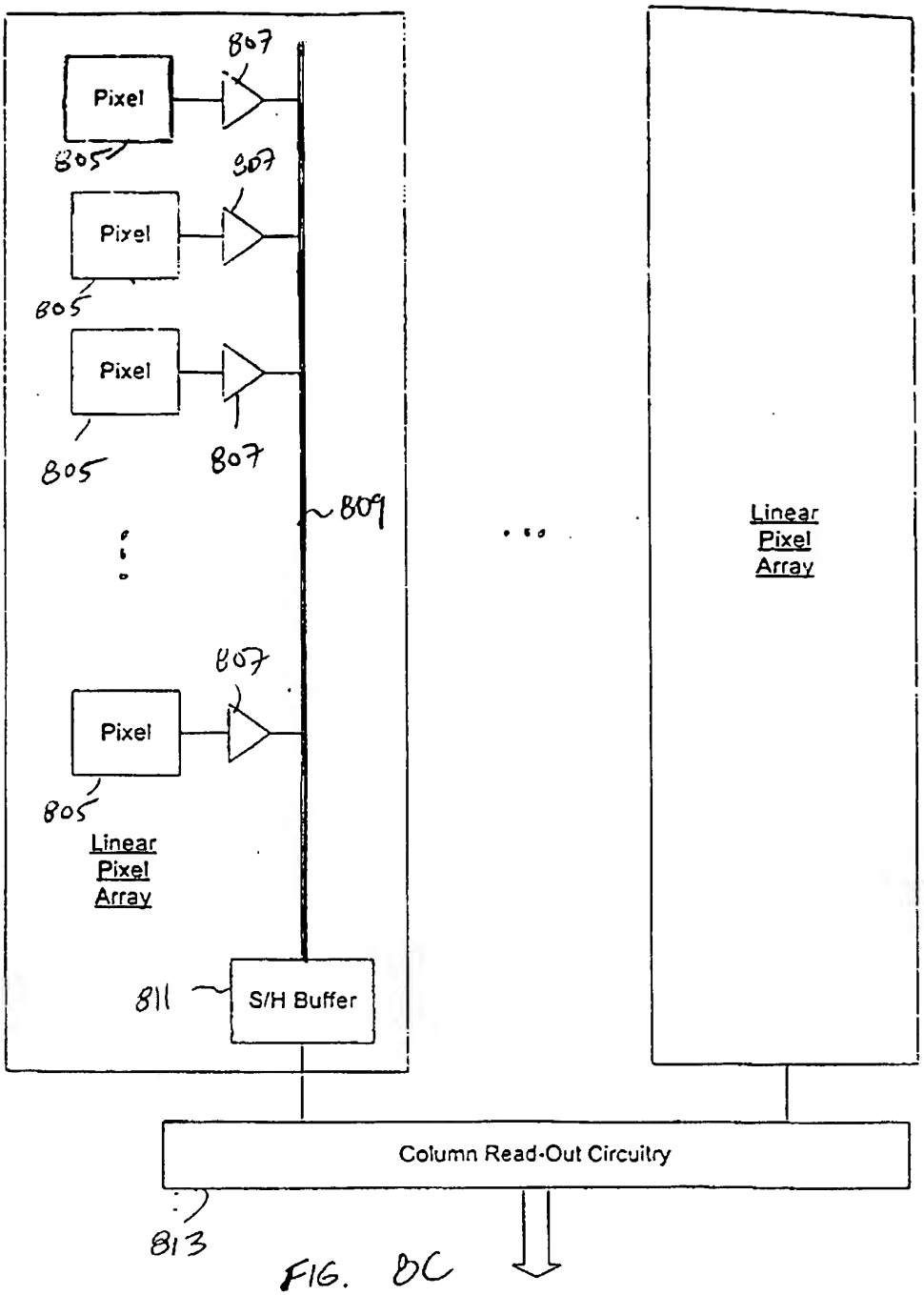

807
Pixel
805
807
Pixel
805
Pixel
805
807
809
807
Pixel
805
Linear
Pixel
Array
811
S/H Buffer
Linear
Pixel
Array
Column Read-Out Circuitry
813

FIG. 8C